LH5P832

CMOS 256K (32K × 8) Pseudo-Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 100/120 ns (MAX.)
- Cycle time: 160/190 ns (MIN.)
- Power consumption:
  Operating: 357.5/303 mW
  Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycle/4 ms
- Auto refresh is executed by internal counter (controlled by $\overline{OE}$/RFSH pin)
- Self refresh is executed by internal timer
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH5P832 is a 256K bit Pseudo-Static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5P832 uses convenient on-chip refresh circuitry with a DRAM memory cell for pseudo static operation. This simplifies external clock inputs, while providing the same simple, non-multiplexed pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, many 32K × 8 SRAM sockets can be filled with the LH5P832 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P832 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low standby power, and a simple interface.

Three methods of refresh control are provided for maximum versatility. A 'CE-Only' refresh cycle refreshes the addressed row of memory cells transparently. All 256 rows must be refreshed or accessed every four milliseconds. 'Auto Refresh' automatically cycles through a different row on every OE/RFSH clock pulse, accomplishing the row refreshes without the need to supply row addresses externally. 'Self Refresh' further simplifies the refresh requirements by eliminating the need for address inputs and clock pulses entirely. An automatic timer senses time periods when memory accesses have ceased, and provides full refresh of all rows of memory without any external assistance.

PIN CONNECTIONS

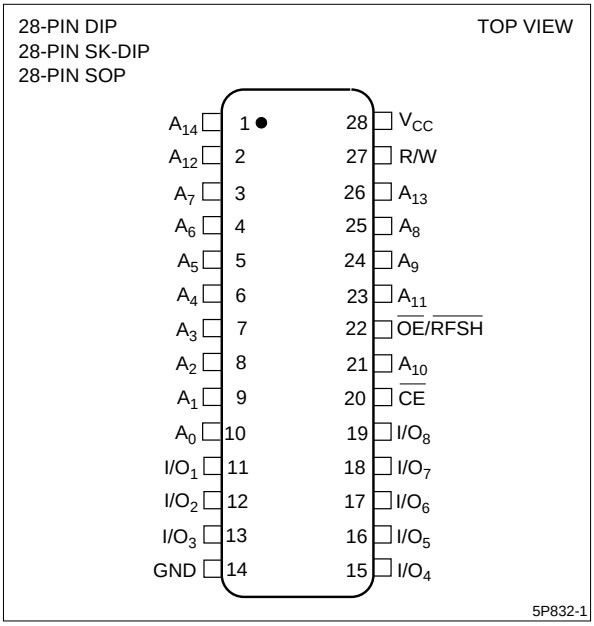


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

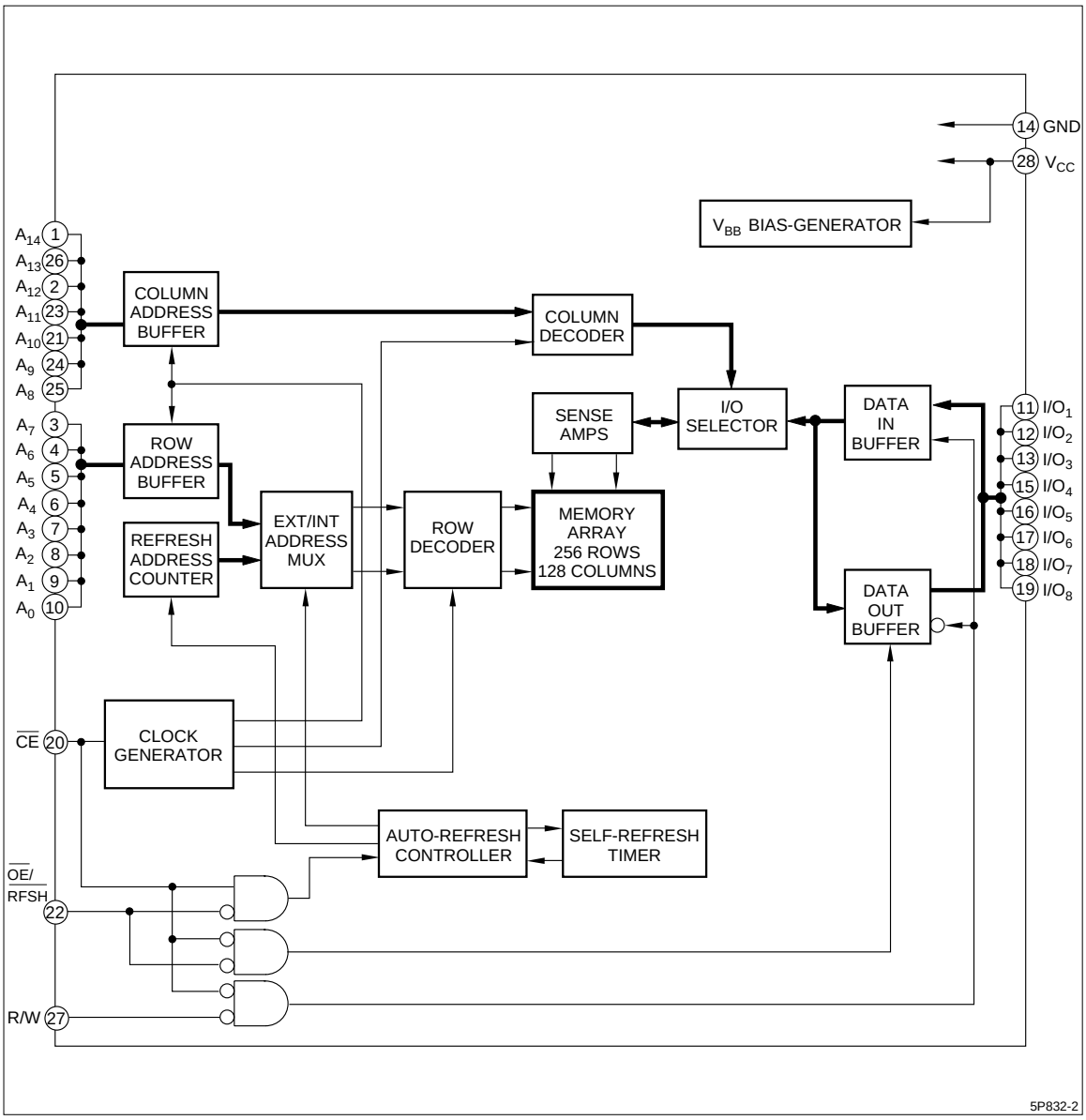


Figure 2. LH5P832 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
R/W	Read/Write input
$\overline{OE}$/RFSH	Output Enable/Refresh input
I/O_1 - I/O_8	Data inputs and outputs
A_0 - A_7	Row address inputs

SIGNAL	PIN NAME
A_8 - A_{14}	Column Address inputs
$\overline{CE}$	Chip Enable input
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	R/W	$\overline{OE}$/$\overline{RFSH}$	MODE	I/O_1 - I/O_8	I_{CC}	NOTE
L	L	X	Write	Data in	Operating (I_{CC1})	1
L	H	L	Read	Data out	Operating (I_{CC1})	
L	H	H	$\overline{CE}$-Only Refresh	High-Z	Operating (I_{CC1})	
H	X	L	Auto Refresh	High-Z	Operating (I_{CC1})	1, 2
H	X	L	Self Refresh	High-Z	Self Refresh (I_{CC3})	1, 3
H	X	H	Standby	High-Z	Standby (I_{CC2})	1

NOTES:
1. X = H or L 2. $\overline{OE}$ Pulsewidth < 8 µs 3. $\overline{OE}$ Pulsewidth ≥ 8 µs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		+0.8	V

CAPACITANCE (V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, f = 1 MHz)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{14}, R/W	C_{IN1}		8	pF
	$\overline{CE}$, $\overline{OE}$/RFSH	C_{IN2}		5	pF
Input/output capacitance	I/O_1 - I/O_8	C_{OUT1}		12	pF

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	I_{CC1}	tRC = 160 ns		65	mA	1, 2
Operating current	I_{CC1}	tRC = 190 ns		55	mA	1, 2
Standby current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/RFSH = V_{IH}		3	mA	1
Self refresh average current	I_{CC3}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/RFSH = V_{IL}		3	mA	1
CPU internal cycle average current	I_{CC4}	tRC = 160 ns		65	mA	1, 2
CPU internal cycle average current	I_{CC4}	tRC = 190 ns		55	mA	1, 2
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V	-10	10	µA	3
Output High voltage	V_{OH}	I_{OUT} = -1 mA	2.4		V	
Output Low voltage	V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:
1. Specified values are with outputs open.
2. I_{CC1} and I_{CC4} depend on the cycle time.
3. The output pins are in high-impedance state.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	5 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL gate, C_L = 100 pF	1

NOTE:
1. Includes scope and jig capacitance.

AC CHARACTERISTICS

READ AND WRITE CYCLES [1,2] (V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	160 ns		190 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	160		190		ns	
Read modify write cycle time	t_{RMW}	225		280		ns	
$\overline{CE}$ pulse width	t_{CE}	100	10,000	120	10,000	ns	
$\overline{CE}$ precharge time	t_P	50		60		ns	
Address setup time	t_{AS}	0		0		ns	
Address hold time	t_{AH}	20		30		ns	
Read command hold time	t_{RCH}	0		0		ns	
Read command setup time	t_{RCS}	0		0		ns	
$\overline{CE}$ access time	t_{CEA}		100		120	ns	3
$\overline{OE}$ access time	t_{OEA}		40		50	ns	3
$\overline{CE}$ to output in Low-Z	t_{CLZ}	10		10		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	30	0	35	ns	2
Output disable to output in High-Z	t_{OHZ}	0	30	0	35	ns	2
Write enable to output in High-Z	t_{WHZ}	0	30	0	35	ns	2
$\overline{OE}$ setup time	t_{OES}	10		10		ns	
$\overline{OE}$ hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ lead time	t_{OEL}	10		10		ns	
Write command pulse width	t_{WCP}	60		85		ns	
Write command setup time	t_{WCS}	60		85		ns	
Write command hold time	t_{WCH}	60		85		ns	
Data setup time from write	t_{DSW}	40		50		ns	
Data setup time from $\overline{CE}$	t_{DSC}	40		50		ns	
Data hold time from write	t_{DHW}	0		0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		0		ns	
Transition time (rise and fall)	t_T	3	35	3	35	ns	
Refresh time interval	t_{REF}		4		4	ms	

REFRESH CYCLE

Auto refresh cycle time	t_{FC}	160		190		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	50		60		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	60	8,000	80	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		ns	
$\overline{CE}$ delay time from refresh active (Auto refresh)	t_{FCE}	190		225		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	190		225		ns	

NOTES:

1. At least 200 µs of pause time after power on should be given for proper device operation.
   $\overline{CE}$ and OE/RFSH must be fixed at V_{IH} for 200 µs from the V_{DD} reached to the specified voltage level
   and followed by at least 8 dummy cycles.
2. AC characteristics are measured at t_T = 5 ns.
3. Measured with a load circuit equivalent to 1TTL loads and 100 pF.

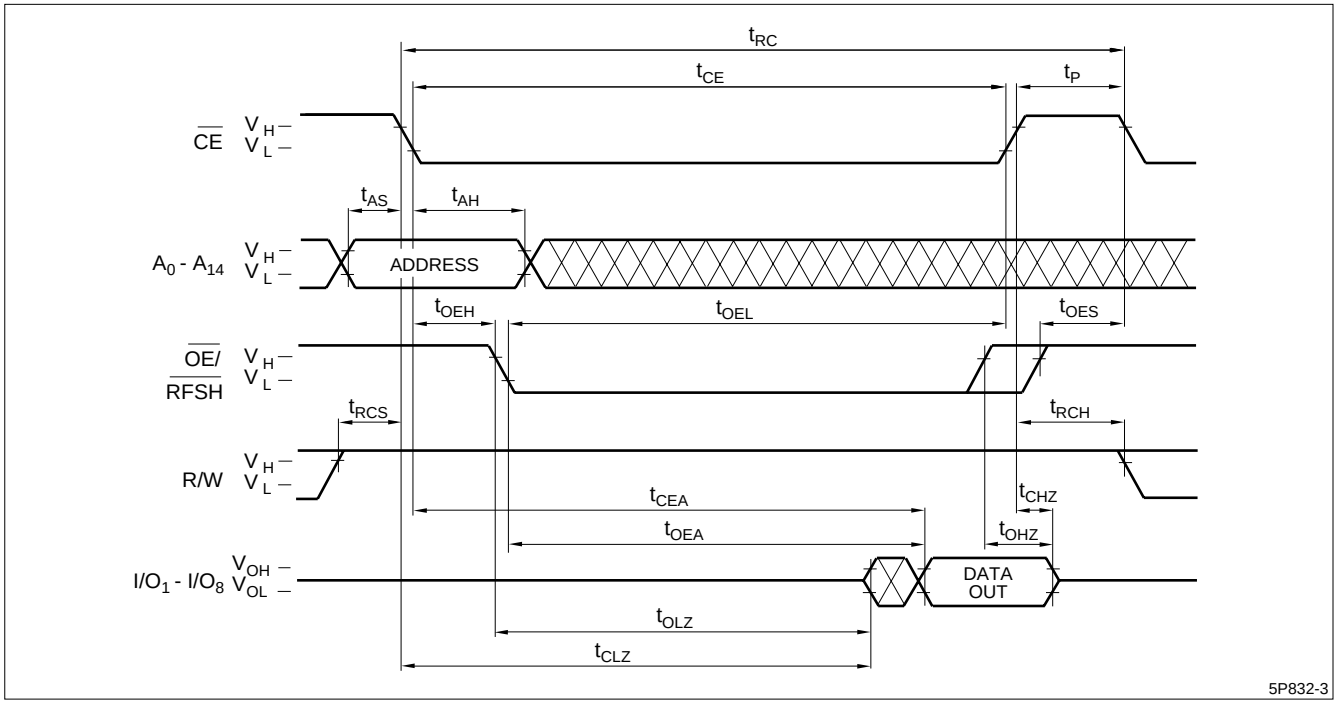


Figure 3. Read Cycle

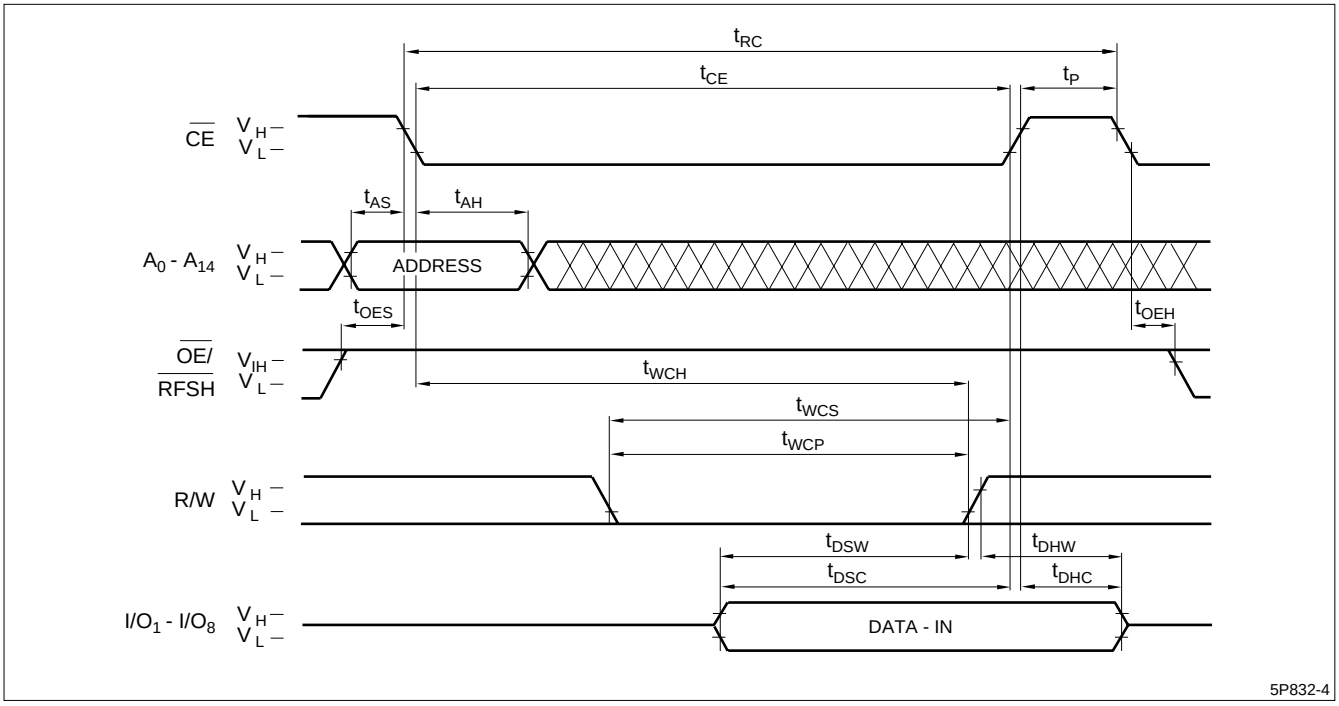


Figure 4. Write Cycle

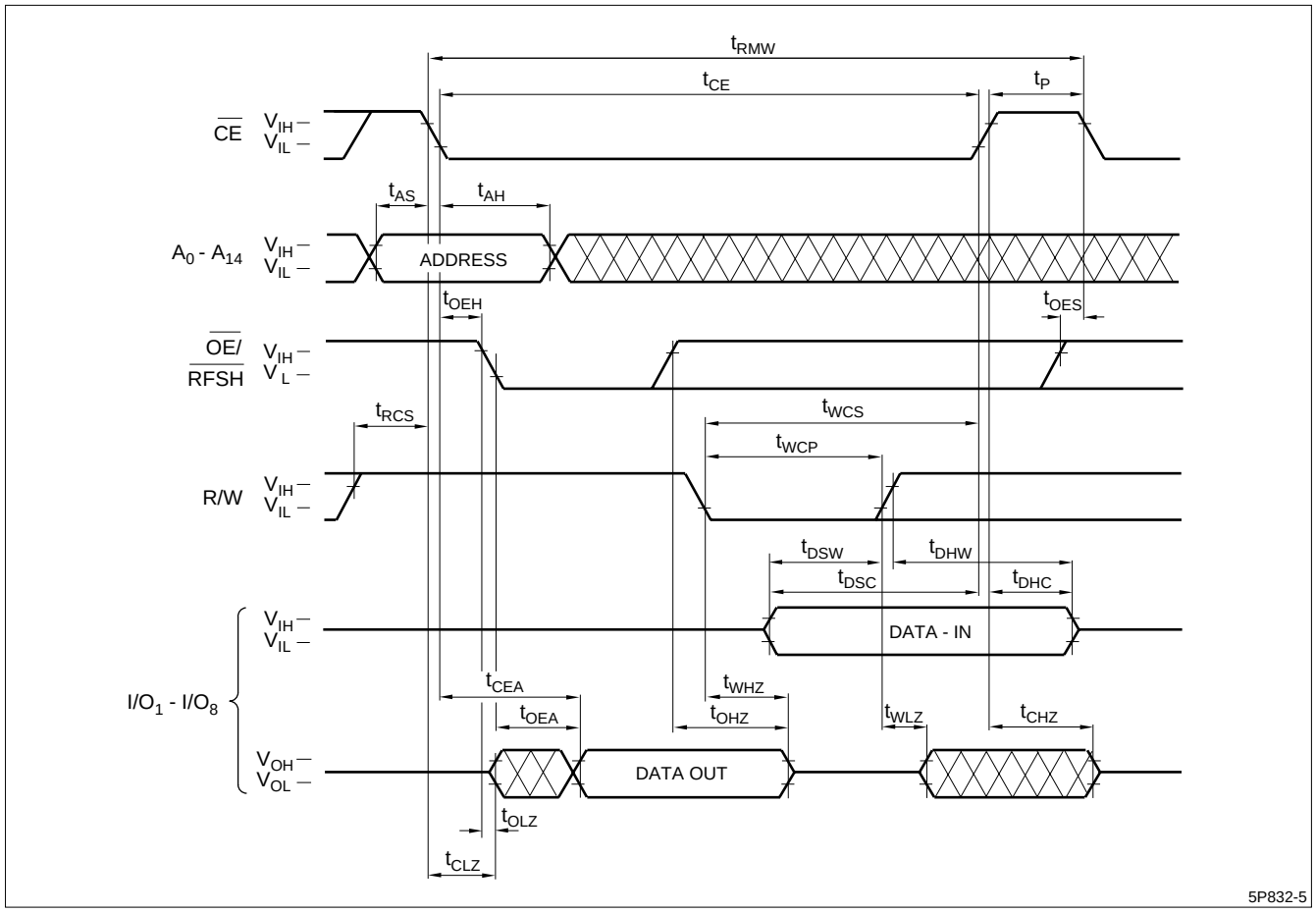


Figure 5. Read/Write Cycle

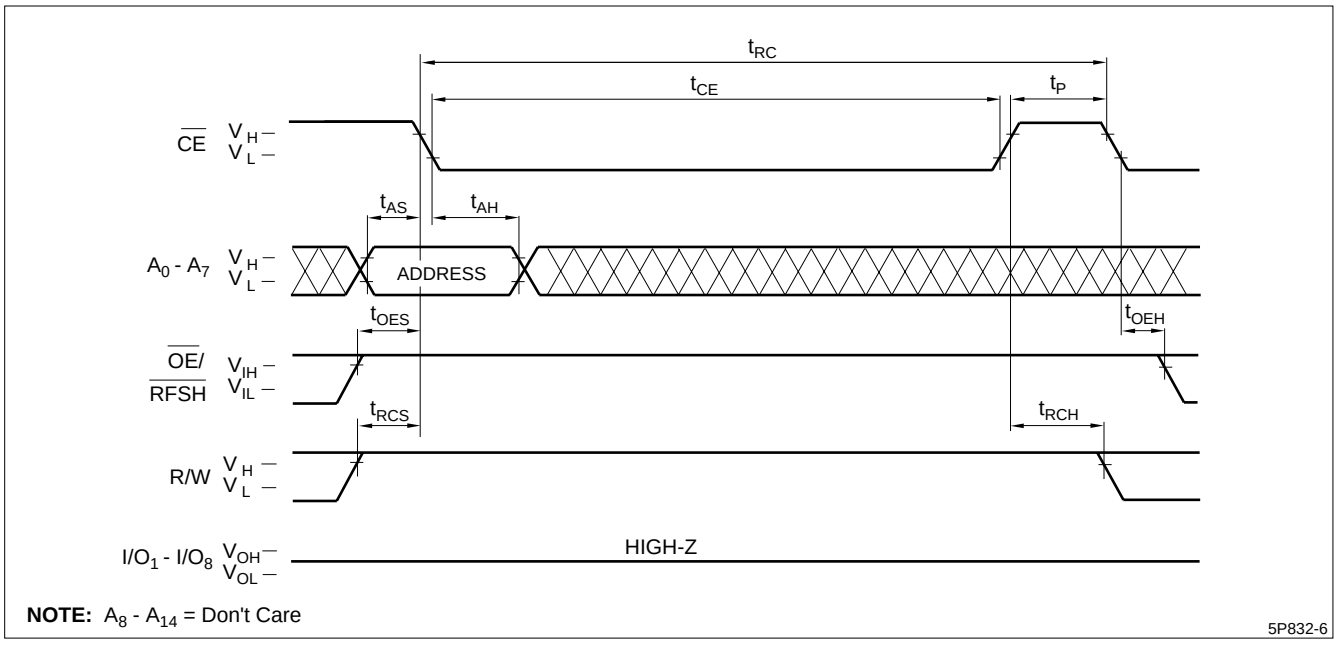


Figure 6. $\overline{CE}$ Only Refresh Cycle

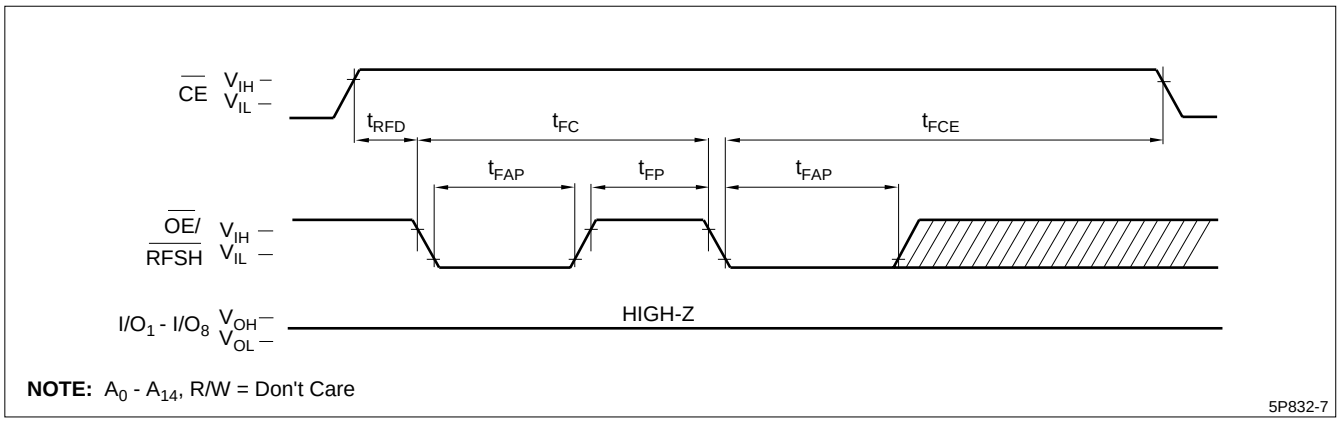


Figure 7. Auto Refresh Cycle

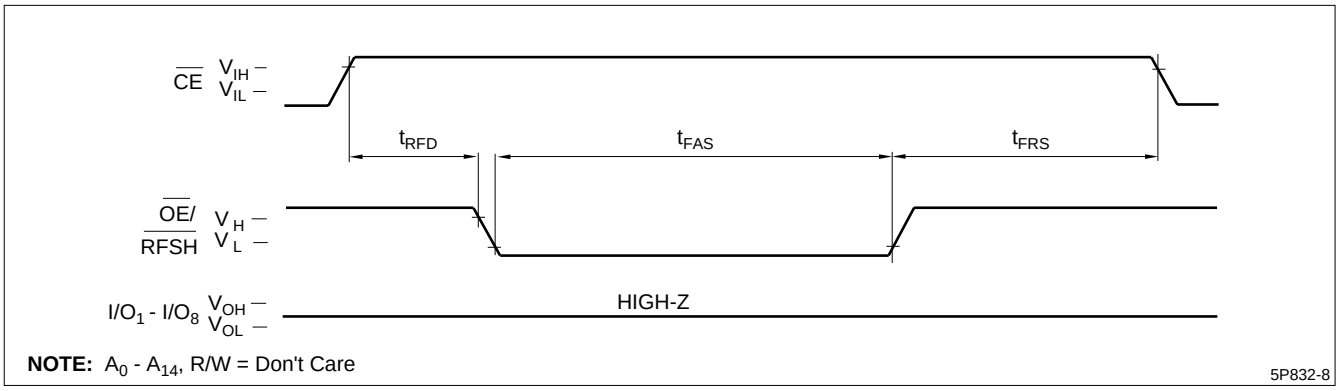
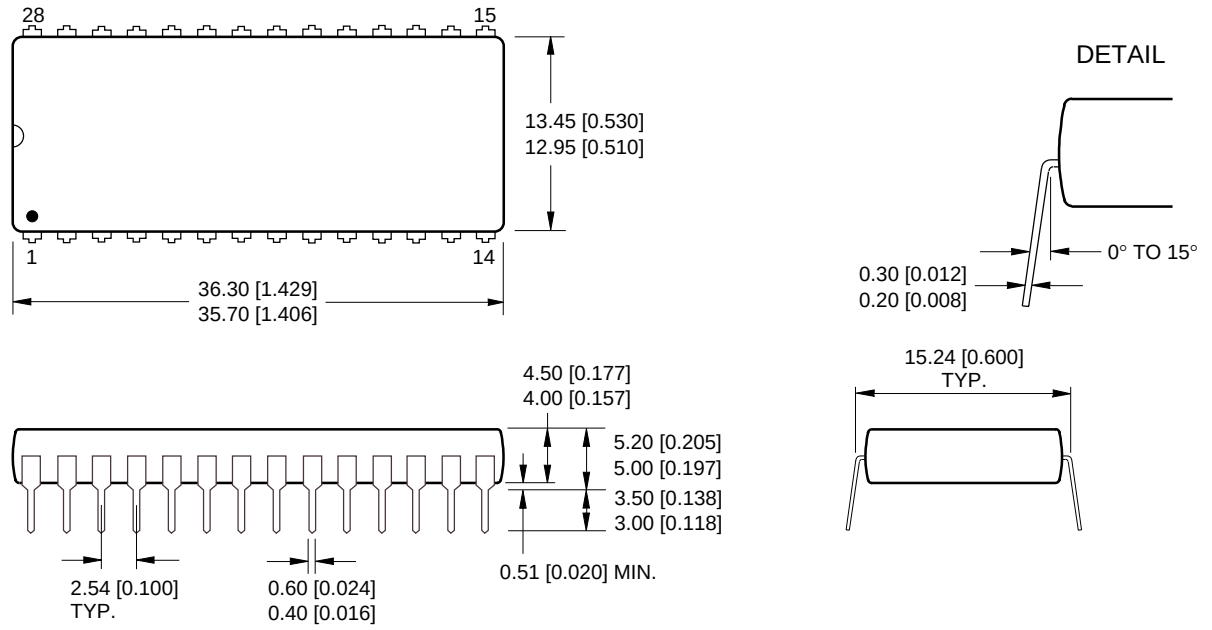


Figure 8. Self Refresh Cycle

PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)

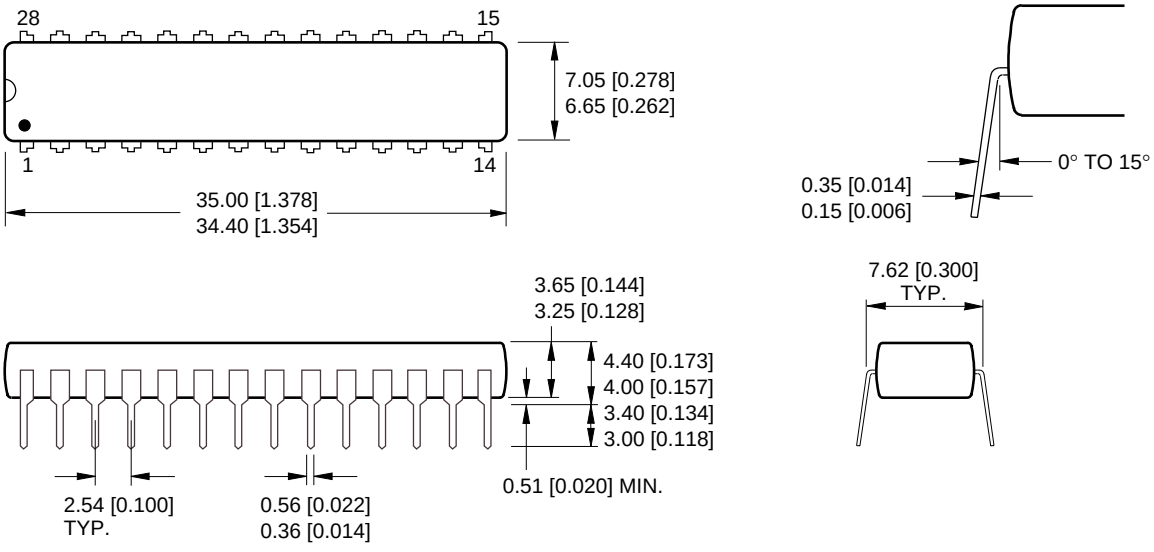


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

28-Pin, 600-mil DIP

28SK-DIP (DIP028-P-0300)

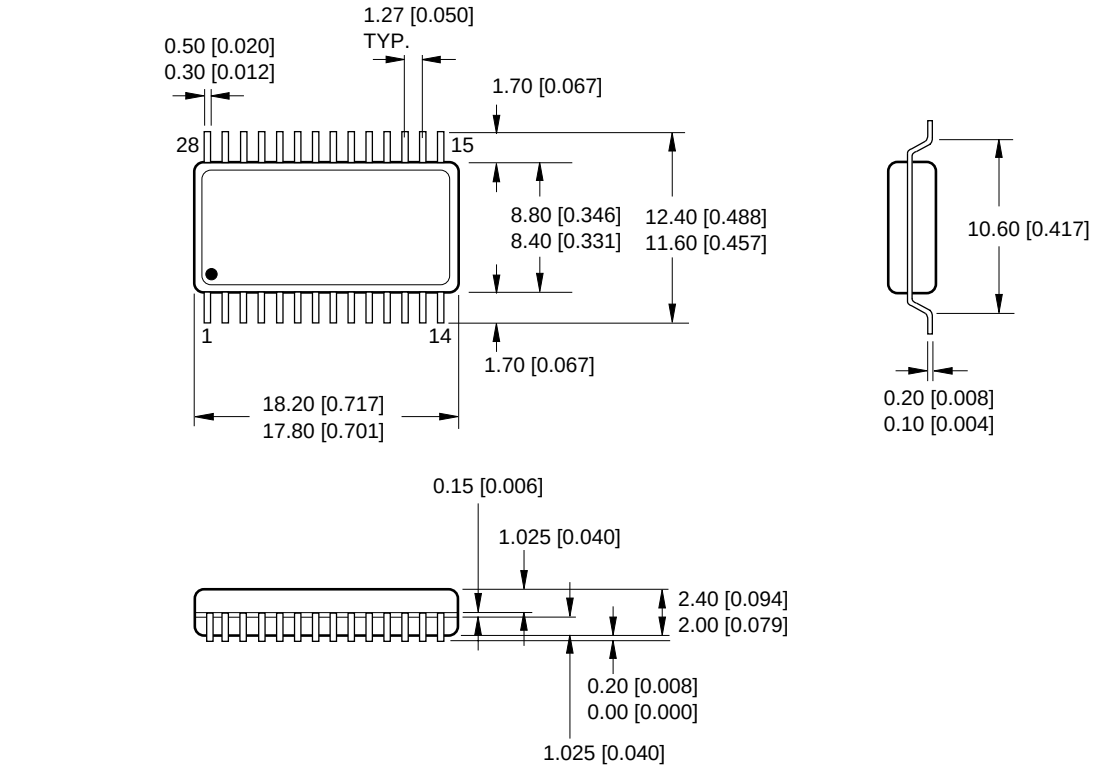


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-1

28-Pin, 300-mil SK-DIP

28SOP (SOP028-P-0450)



28-Pin, 450-mil SOP

ORDERING INFORMATION